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Design and Development of ADIOS Based Pulse Input Counter Module for MPROGICON – 5000 PLC SYSTEMS

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A B S T R A C T

The Pulse input counter module is an enhancement of the MPROGICON-5000 series PLC systems which comprises analog and digital input & output modules. The design is purely based on Modular ADIOS bus, which shall accept pulses in the range of 1Hz to 10 KHz with a time base parameter. The counter status, bus access and fault indication will be provided by front panel LED's. The counter module will include 5 independent channels; each channel can be operated at either 5 or 24 VDC pulse input signals.

Introduction:

In current scenario companies took advantage of automation to stay alive and competitive by automating simple and complex tasks across applications which there by saves time and costs, in turn increases business and IT process reliability and speed while reducing the possibility of human error. Automation applications focus mainly on control technology, in earlier days the engineer completely relied on power relays to develop automation applications. The substantial economic growth, however, raise in mass production and the weight of quality are concern for engineers involved in the development of control technologies. As part of this change in focus, non- programmable logic controllers were developed. But automation engineers soon discovered that the non-programmable nature of these devices made it hard to design a truly automatic system. For this reason, the PLC (Programmable Logic Controller) was invented. PLCs were set up to operate both independently as well as were design to operate with a console port to connect to a computer for configuration purposes. A Programmable logic controller is a user-friendly electronic computer that carries out control functions of many types and levels of complexity. It can be controlled, programmed and operated by a person unskilled in operating computers. The major parts of PLC are Central Processing Unit, Monitor, and I/O modules. The CPU is the heart of the PLC system. The Input-output modules include analog, digital, pulse input, thermo-couple modules. As technology progresses the requirement of different application specific I/O modules increased and Invention of newer protocols, newer communication technologies do take place. So there is need to upgrade the I/O modules in a PLC as and when necessary to enhance its performance

Pulse Counter Module:

Pulse Counter Module is integrated into MPROGICON-5000 series PLC has 5 independent channels operated at either 5V or 24V DC. Each channel shall have one digital input (IN_AUX), pulse input (IN_A) and one discrete output is shown in Fig: 1

A. Pulse Input (IN_A):

Fig: 1. Basic Block Diagram of Channel

PULSE COUNTER MODULE is designed electrically and mechanically compatible with ADIOS bus. The ADIOS bus based PULSE COUNTER MODULE accepts the pulses from outside field devices (Counter inputs). The outside devices that shall operate on 60V, 1.5A (max) shall be interfaced with this board. The pulse input board consists of five independent counters, in other words this board can accepts maximum of five channel inputs (outside devices). The

counter status, bus access and fault indication will be provided by front panel LED's. The counter output protection will be provided through 500 mA resettable fuses. Counter accepts up to 1 to 10 KHz. Each Counter can be operated in four modes which can be configured logically. PULSE COUNTER MODULE has a 16-bit address and data computing capability with interface to ADIOS bus. The module incorporates an ADIOS bus interface to communicate with other ADIOS bus compatible devices such as CPU boards, serial I/O controllers, and disk controllers. The MODULE is compatible with l6-bit data, or 16 bit address, ADIOS bus compatible devices, but maximum performance will be obtained when ECCM5700 operated in a 16 bit address and data or ADIOS bus environment. The simplified block diagram of PULSE COUNTER MODULE is shown in Fig: 2.

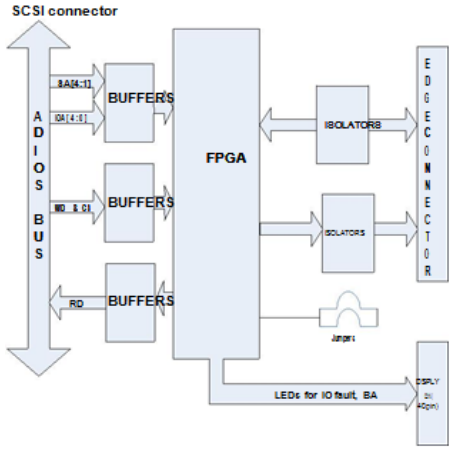

Fig: 2. Design Architecture of Pulse Counter Module

Edge Connector: This Edge connector feeds inputs to counters with incoming frequency/pulses ranging from 0-10KHz and the digital input of 5V or 24V DC.

Isolators: These isolators are used in order to achieve channel to channel isolation electrically.

FPGA: The FPGA acts as an interface between field and ADIOS bus.

Buffers: These buffers are used to drive FPGA signals to the bus and bus signals to FPGA.

WD [15:0]: For the selected address of the board the host CPU can write data into pulse input module through Write data port WD [15:0].

RD [15:0]: 16-bit value read back from the selected Outputs Group indicating their current status.

SA [3:0]: This is I/O bus motherboard contains 18/10 slots for 512/256 I/O configurations. Each slot is selected with appropriate jumpers. Installing a jumper the slot select line gives '0' level, jumper not installed the slot select line gives '1' level.

IOA [4:0]: where the pulse input module will have a 4-bit unique board address as set on the motherboard for the I/O slot.

CS: This represents 3-bit code indicating the type of the board present in the selected slot

SCSI: This is a 100-pin right angled male connector used in the pulse input module so that the module can be mounted on to the bus.

B. Operating Modes of ECM5700:

The ADIOS based Pulse input board operating modes are

- Event-Up Counting mode
- Event-Down Counting mode
- Period measurement mode
- Rate Counter mode

ADIOS BUS Interfaces:

The data transfer protocol has been developed based on 16-bit special function registers .which are implemented in FPGA of the module. The special functions registers in ECM5700 like Global configuration register (GCR), Local Configuration register (LCR) , Initial value register (IVR), Preset/ Target Value Register (PVR/TVR) , Current Value register (CVR), Counter Status register (CSR).which will be used to configure, control and operate the module.

Proposed Protocol:

The 16-bit data write & read special function registers defined in FPGA of Module are configured by write operation through Write Data Port WD [15:0] when WDEN is asserted and also can be read through Read data Part RD [15:0] by the host CPU when RDEN is asserted through ADIOS interface. Global configuration register is read & write register that contains valid bits in lower byte of D [15:0] that

- Enables/disables all the five channels
- Set/Reset all the five channels

Local configuration register is read & write register contains valid bits in lower byte of D [15:0] that

- Enables/disables a particular channel
- Set/reset particular channel
- Set a channel to run in available operating modes

Initial value register holds valid 16 bits D [15:0] that conveys channel to start counting from that initial value. By default initial value of IVR=' 0000H '. Pre-set / Target Value register holds 16 bits that are used to set a particular counter with pre-set/target value i.e. where counter should stop counting, By default initial value of PVR='FFFFH'. The value in IVR and PVR gets cleared only due to power

ON reset or board reset and doesn't get affected due to the reset bit mentioned in GCR & LCR in module. Current Value register is read-only register that contains 16 bits in

D [15:0] that is used to read counter's current value in pulse input module. Current Status register is read-only register that holds valid 16 bits in lower byte & higher byte of D [15:0] that allows user to recognise current status of particular counter in pulse input module. The figure 3 shows the test setup for the ECM5700

performance.

Operation of Circuitry in Pulse Counter Module

Major Components:

- Voltage regulator(LM1085)
- Hot swap(TPS2421)
- Reset Circuit (DS1834)
- Optocoupler (ACPL217)
- FPGA (LFXP25QN208)
- Crystal Oscillator
- Solid State Relays (AQV102A)
- Buffers
- **Solid state relays :**
  Principle: It is an electronic switching device where a small signal controls a large load current/voltage.

  Preferred: Faster than electro-mechanical relays,

  Has less electrical noise,

  No sparkling effects.

- **Optocoupler :**
  Principle: Within electronic circuit equipment there are some situations where data signals have to be transferred from source (input from field) to destination (FPGA) and FPGA can't take 230V

- **Voltage Regulator :**
  Principle: It regulates bus supply voltage 5V DC to 3.3VDC

- **Buffers :**
  Principle: buffers are used to drive FPGA signals to the bus and bus signals to FPGA to accept inrush current

- **Hot Swap:**
  Principle: The circuit uses a FET which switches ON with discharge of coupling capacitor to accept inrush current

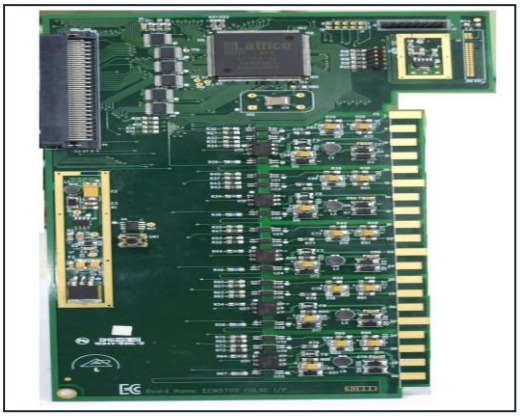

Fig. 3: ECM5700 Circuit Board

A. Counter-N in Operating Mode-Xxx Algorithm Simulation Results:

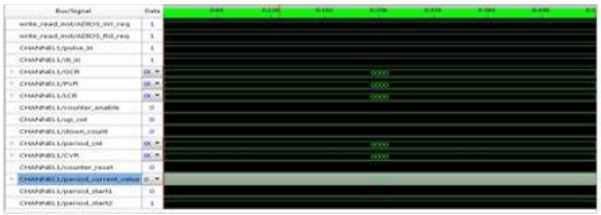

Fig. 4: reveal logic analyzer waveform

Fig. 5: reveal logic analyzer waveform2

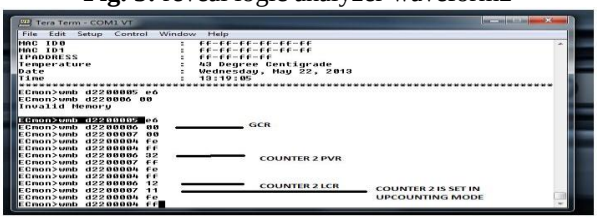

Fig. 6: Results set1 in Teraterm

Fig. 7: Results set2 in Teraterm

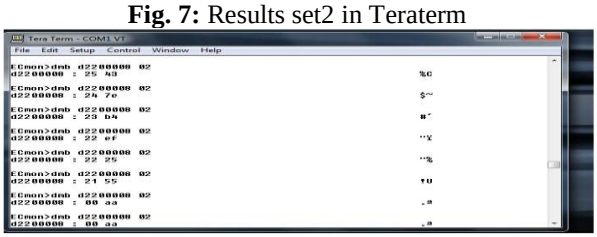

Fig. 8: Results set3 in Teraterm

The figures 4 and 5 show the relative waveforms of reveal logic analyzer at different intervals. Figure 6, 7 and 8 depicting the results in teratem at different levels.

Conclusion:

The ADIOS Bus Interface between CPU and Pulse Counter Module is completed. The Interface is implemented in Verilog HDL. The code is synthesized and programmed into a FPGA using Lattice Diamond software. The design of ECM5700 is complete and presently tested by loading the test applications.

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